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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,796	03/23/2004	Martin Langhammer	15114H-073600US	4384

26059 7590 07/23/2007

TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
YAARY, MICHAEL D	
ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
07/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,796	LANGHAMMER, MARTIN	
	Examiner	Art Unit	
	Michael Yaary	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-32 are pending in the application.

2. The title is not descriptive, a new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise as it fails to disclose what the digital signal processor is accomplishing.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 8-12, 14, 18, 21-26, and 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bosshart (US Pat. 4,754,421) in view of Lee (US Pat. 6,460,064).

5. **As to claim 1 and 14,** Bosshart discloses a multiplication unit, having a first short word length multiplication mode and a second long word length multiplication mode (abstract), wherein:

In the first mode, a first long word length multiplicand is formed from a first short word length multiplicand, a second long word length multiplicand is formed from a

second short word length multiplicand, and the first and second long word length multiplicands are multiplied together to form a result which includes the product of the first and second short word length multiplicands (column 1, line 58-column 2, line 12; and column 4, lines 58-63), and first and second words being stored in registers (column 2, lines 3-12).

6. Bosshart does not disclose in the second mode, wherein a third long word length multiplicand is formed from a first pair of short word length words and a fourth pair long word length multiplicand is formed from a second pair of short word length words, and subsequently the third and fourth long word length multiplicands are multiplied together.

However, Lee discloses in the second mode, wherein a third long word length multiplicand is formed from a first pair of short word length words and a fourth pair long word length multiplicand is formed from a second pair of short word length words, and subsequently the third and fourth long word length multiplicands are multiplied together (column 2, line 59-column 3, line 24 and column 4, lines 52-65).

7. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bosshart by, forming long word length multiplicands from short word length words, as taught by Lee, for the benefit of being able to avoid slow operation speed while at the same time maintaining relatively small circuit size in a multiplier circuit.

8. **As to claims 5 and 18,** Bosshart further discloses in the second mode, second words of the first and second pair of short word length words are stored in respective registers, before the third and fourth long word length multiplicands are multiplied together (column 2, lines 3-12 and column 2, line 60-column 3, line 21).

9. **As to claim 26,** the claim is rejected for the same reasons as claims 1 and 14 above and in addition Lee discloses the second length is twice the first length (column 2, lines 64-67).

10. **As to claims 8, 21, and 28,** Bosshart further discloses first and second long word accumulators, for receiving the multiplication results (column 3, lines 2-8).

11. **As to claims 9, 22, and 29,** Bosshart further discloses in the second mode, the result of multiplying together third and fourth long word length multiplicands can be divided between the first and second long word accumulators (column 3, lines 2-8 and column 4, lines 25-54).

12. **As to claims 10, 23, and 30,** Bosshart further discloses in the second mode, a selected part of the result of multiplying together the third and fourth long word length multiplicands can be stored in a selected one of the first and second long word length accumulators (column 3, lines 2-8 and column 4, lines 25-54).

13. **As to claims 11, 12, 24, 25, 31, and 32** Lee discloses the short word length is 16 bits and the long word length is 32 bits (column 2, lines 64-67 disclose multiplying using n bits and n/2 bits thus making it obvious that 16, 18, 32, 36, or even 64 bits can be used.).

14. Claims 2-4, 13, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bosshart in view of Lee as applied to claim 1 above, and further in view of Yu et al. (hereafter Yu)(US Pat. 6,523,055).

15. **As to claims 2 and 15,** Bosshart and Lee do not disclose in the first mode, the first long word length multiplicand is formed as a sign extended version of the first short word length multiplicand, and the second long word length multiplicand is formed as a sign extended version of the second short word length multiplicand.

However, Yu discloses in the first mode, the first long word length multiplicand is formed as a sign extended version of the first short word length multiplicand, and the second long word length multiplicand is formed as a sign extended version of the second short word length multiplicand (column 6, line 54-column 7, line 7 and column 8, lines 31-40).

16. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bosshart and Lee, by sign extending the multiplicands, as taught by Yu, for the benefit of being able to utilize less hardware in a multiplier circuit.

17. **As to claims 3 and 16,** Yu discloses in the first mode, the first long word length multiplicand is formed from the first short word length multiplicand plus zeroes as the most significant bits, and the second long word length multiplicand is formed from the second short word length multiplicand plus zeroes as the most significant bits, such that the multiplication result includes an unsigned product of the first and second short word length multiplicands (column 6, lines 54-61).

18. **As to claims 4 and 17,** Yu discloses in the first mode, the first long word length multiplicand is formed from the first short word length multiplicand plus zeros as the least significant bits, and the second long word length multiplicand is formed from the second short word length multiplicand plus zeroes as the least significant bits, such that upper bits of the multiplication result contain the product of the first and second short word length multiplicands (column 6, lines 54-61).

19. **As to claim 13,** the claim is rejected for the same reasons as claims 1 and 3 above.

20. Claims 6, 7, 19, 20, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bosshart and Lee as applied to claim 1 above, and further in view of Henderson et al. (hereafter Henderson)(US Pat. 6,484,194).

21. **As to claims 6, 7, 19, 20, and 27,** Bosshart and Lee do not disclose a register file, from which the first and second short word length multiplicands, and the first and second pairs of short word length words can be retrieved; and the register file is a dual ported register file, such that: in the first mode, the first and second short word length multiplicands can be retrieved at the same time, and in the second mode, first words of the first and second pairs of short word length words can be retrieved at a first time, and second words of the first an second pairs of short word length words can retrieved at a second time.

However, Henderson discloses a register file, from which the first and second short word length multiplicands, and the first and second pairs of short word length words can be retrieved; and the register file is a dual ported register file, such that: in the first mode, the first and second short word length multiplicands can be retrieved at the same time, and in the second mode, first words of the first and second pairs of short word length words can be retrieved at a first time, and second words of the first an

second pairs of short word length words can retrieved at a second time (Column 13, lines 39-61 disclose a dual ported register file that enable addressing and access to two operands when words are read, thus being able to different word sets at the same time).

22. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bosshart and Lee, by implementing a dual ported register file, as taught by Henderson, for the benefit of maintaining a fast execution time in the multiplier circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Yaary whose telephone number is (571) 270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MY

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100